Задание 1. Переведите предложения, содержащий термины и аббревиацию. Запишите перевод ТОЛЬКО терминов/аббревиации, выделенных жирным шрифтом в именительном падеже (см. «Критерии оценивания»).

True (1) **CDP** backup write operations are executed at the level of BIOS of the microcomputer in such a manner that normal use of the computer is unaffected.
(2) **GEM** provides an (3) **API** with explicit memory management primitives.
The main concept of (4) **TTM** are the «buffer objects», regions of video memory that at some point must be addressable by the (5) **GPU**.
Originally, (6) **EEPROM**s were limited to single-byte operations, which made them slower, but modern EEPROMs allow multi-byte page operations.
*(*7) **FLOPS** can be recorded in different measures of precision, for example, the TOP500 supercomputer list ranks computers by 64-bit operations per second, abbreviated to *FP64*.
One aim of the (8) **IDE** is to reduce the configuration necessary to piece together multiple development utilities.
The performance of an (9) **ADC** is primarily characterized by its bandwidth and signal-to-noise ratio.
One of the organizational units of (10) **JVM** byte code is a class.

Задание 2. Прочитайте текст на английском языке и сделайте пересказ текста на русском языке. Прочитайте текст на английском языке и сделайте пересказ текста на русском языке. Объем русского текста должен быть 150-160 слов. Текст, объем которого меньше 135 или больше 180 слов, не проверяется.

Scrolling is the movement of the displayed portion of the map. Games scroll to show an area much larger than the 256x240 pixel screen. For example, areas in *Super Mario Bros.* are many screens wide. The NES's first major improvement over its immediate predecessors was pixel-level scrolling of playfields.

Ordinarily, a program writes to two PPU registers to set the scroll position in its NMI handler:

Find the 9-bit X and Y coordinates of the upper left corner of the visible area (the part seen by the «camera»)

Write the lower 8 bits of the X coordinate to PPUSCROLL ($2005)

Write the lower 8 bits of the Y coordinate to PPUSCROLL

Write the 9th bit of X and Y to bits 0 and 1, respectively, of PPUCTRL ($2000). This is the nametable that’s visible in the top-left corner.

The scroll position written to PPUSCROLL is applied at the end of vertical blanking, just before rendering begins, therefore these writes need to occur before the end of vblank. Also, because writes to PPUADDR ($2006) can overwrite the scroll position, the two writes to PPUSCROLL and the write to PPUCTRL must be done after any updates to VRAM using PPUADDR.

By itself, this allows moving the camera within a usually two-screen area (see Mirroring), with horizontal and vertical wraparound if the camera goes out of bounds. To scroll over a larger area than the two screens that are already in VRAM, you choose appropriate offscreen columns or rows of the nametable, and you write that to VRAM before you set the scroll, as seen in the animation below. The area that needs rewritten at any given time is sometimes called the «seam» of the scroll.

Frequent pitfalls

Don’t take too long

If your NMI handler routine takes too long and PPUSCROLL ($2005) is not set before the end of vblank, the scroll will not be correctly applied this frame. Most games do not write more than 64 bytes to the nametable per NMI; more than this may require advanced techniques to fit this narrow window of time.

Set the scroll last

After using PPUADDR ($2006), the program must always set PPUCTRL and PPUSCROLL again. They have a shared internal register and using PPUADDR will overwrite the scroll position.

If the screen does not use split-scrolling, setting the position of the background requires only writing the X and Y coordinates to $2005 and the high bit of both coordinates to $2000.

Programming or emulating a game that uses complex raster effects, on the other hand, requires a complete understanding of how the various address registers inside the PPU work.

Here are the related registers:

v - Current VRAM address (15 bits)

t - Temporary VRAM address (15 bits); can also be thought of as the address of the top left onscreen tile.

x - Fine X scroll (3 bits)

w - First or second write toggle (1 bit)

The PPU uses the current VRAM address for both reading and writing PPU memory thru $2007, and for fetching nametable data to draw the background. As it's drawing the background, it updates the address to point to the nametable data currently being drawn. Bits 10-11 hold the base address of the nametable minus $2000. Bits 12-14 are the Y offset of a scanline within a tile.